Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a data processing system for isolating a defect in a memory system ~~to a particular memory system component~~, said method comprising the steps of:

said memory system including ~~a plurality of components, said plurality of components including~~ a memory card, a plurality of physical dual inline memory modules (DIMMs) that are attached ~~coupled~~ to said [[a]] memory card, ~~said memory card,~~ and a memory controller for controlling said memory card; [[and]]

said memory card coupled to said memory controller using a JTAG bus, said memory card including a plurality of empty slots to which additional physical DIMMs can be attached, and said memory card including a plurality of electrical buffers that are part of said memory card;

testing said plurality of physical DIMMs first using a physical DIMM test;

responsive to no error occurring during said physical DIMM test, testing said memory card using a memory card test;

responsive to no error occurring during said memory card test, testing said memory controller next using a memory controller test;

responsive to said memory controller passing said memory controller test, determining that said memory system is good;

utilizing said plurality of electrical buffers as a virtual memory controller when testing said plurality of physical DIMMs, and utilizing said plurality of electrical buffers as virtual physical DIMMs when testing said memory card;

coupling said plurality of electrical buffers to a service processor using a JTAG bus, said service processor controlling said plurality of electrical buffers using said JTAG bus;

said physical DIMM test including:

scanning DIMM test data and address information to said plurality of electrical buffers, which then scan said DIMM test data to all addresses in each one of said plurality of physical DIMMs;

reading data from said plurality of physical DIMMs;

scanning, from said plurality of electrical buffers, said data that was read from said plurality of physical DIMMs;

determining that said plurality of physical DIMMs passed said physical DIMM test if said data that was read from said plurality of physical DIMMs matches said DIMM test data;

said memory card test including:

assigning a unique identifier to each one of said plurality of electrical buffers, each one of said plurality of electrical buffers addressable by the service processor using said unique identifier;

treating each one of said plurality of electrical buffers as a virtual physical DIMM;

testing, by the service processor, data bits by writing card test data to each memory location in said virtual physical DIMM, and then reading data from each memory location in said virtual physical DIMM;

if said data that was read from said virtual physical DIMM matches said card test data, performing address bit verification on said memory card;

said address bit verification to test address bits including:

writing a known test pattern to a first memory location that falls within a range of said virtual physical DIMM, and then reading a set of addresses that fall within said range of said virtual physical DIMM;

determining whether said known test pattern was read from only said first memory location;

if said known test pattern was read from only said first memory location: said service processor determining that said memory card passed said address bit verification for said first memory location, removing said known test pattern from said first memory location, and performing said address bit verification on a next memory location; and

if all memory locations that fall within said range pass said address bit verification, determining that said memory card passed said memory card test.

~~testing each one of said plurality of components separately to identify a defective one of said plurality of components.~~

2-8. (Canceled)

9. (Currently amended) The method according to claim 1 [[2]], further comprising the steps of:

storing a controller data pattern in said memory controller;

reading a data pattern from said memory controller;

comparing said controller data pattern ~~written to said memory controller~~ to said data pattern that was read from said memory controller;

determining that said memory controller passed said test in response to said controller data pattern ~~written to said memory controller~~ being the same as said data pattern that was read from said memory controller; and

determining that said memory controller failed said memory controller test in response to said controller data pattern ~~written to said memory controller~~ being different from said data pattern that was read from said memory controller.

10. (Original) The method according to claim 9, further comprising the steps of:
coupling said memory controller to a service processor.

11. (Original) The method according to claim 9, further comprising the steps of:
coupling said memory controller to a service processor utilizing a JTAG bus.

12-13. (Canceled)

14. (Currently amended) A data processing system for isolating a defect in a memory system to a particular memory system component, said system comprising:

said memory system including a memory card, a plurality of physical dual inline memory modules (DIMMs) that are attached to said memory card, and a memory controller for controlling said memory card;

said memory card coupled to said memory controller using a JTAG bus, said memory card including a plurality of empty slots to which additional physical DIMMs can be attached, and said memory card including a plurality of electrical buffers that are part of said memory card;

testing means for testing said plurality of physical DIMMs first using a physical DIMM test;

responsive to no error occurring during said physical DIMM test, testing means for testing said memory card using a memory card test;

responsive to no error occurring during said memory card test, testing means for testing said memory controller next using a memory controller test;

responsive to said memory controller passing said memory controller test, determining means for determining that said memory system is good;

said plurality of electrical buffers utilized as a virtual memory controller when testing said plurality of physical DIMMs, and said plurality of electrical buffers utilized as virtual physical DIMMs when testing said memory card;

coupling said plurality of electrical buffers to a service processor using a JTAG bus, said service processor controlling said plurality of electrical buffers using said JTAG bus;

said physical DIMM test including:

scanning means for scanning DIMM test data and address information to said plurality of electrical buffers, which then scan said DIMM test data to all addresses in each one of said plurality of physical DIMMs;

reading means for reading data from said plurality of physical DIMMs;

scanning means for scanning, from said plurality of electrical buffers, said data that was read from said plurality of physical DIMMs;

determining means for determining that said plurality of physical DIMMs passed said physical DIMM test if said data that was read from said plurality of physical DIMMs matches said DIMM test data;

said memory card test including:

a unique identifier assigned to each one of said plurality of electrical buffers, each one of said plurality of electrical buffers addressable by the service processor using said unique identifier;

each one of said plurality of electrical buffers treated as a virtual physical DIMM;

the service processor testing data bits by writing card test data to each memory location in said virtual physical DIMM, and then reading data from each memory location in said virtual physical DIMM;

if said data that was read from said virtual physical DIMM matches said card test data, performing means for performing address bit verification on said memory card;

said address bit verification to test address bits including:

writing means for writing a known test pattern to a first memory location that falls within a range of said virtual physical DIMM, and then reading means for reading a set of addresses that fall within said range of said virtual physical DIMM;

determining means for determining whether said known test pattern was read from only said first memory location;

if said known test pattern was read from only said first memory location: said service processor determining that said memory card passed said address bit verification for said first memory location, removing said known test pattern from said first memory location, and performing said address bit verification on a next memory location; and

if all memory locations that fall within said range pass said address bit verification, determining means for determining that said memory card passed said memory card test.

~~said memory system including a plurality of components, said plurality of components including a physical memory module coupled to a memory card;~~

~~said memory card, and a memory controller for controlling said memory card; and~~

~~logic that tests each one of said plurality of components separately to identify a defective one of said plurality of components.~~

15-20. (Canceled)

21. (Currently amended) The system according to claim 15, further comprising:

storing means for storing a controller data pattern in said memory controller;

reading means for reading a data pattern from said memory controller;

comparing means for comparing said controller data pattern ~~written to said memory controller~~ to said data pattern that was read from said memory controller;

determining means for determining that said memory controller passed said test in response to said controller data pattern written to said memory controller being the same as said data pattern that was read from said memory controller; and

determining means for determining that said memory controller failed said memory controller test in response to said controller data pattern written to said memory controller being different from said data pattern that was read from said memory controller.

22. (Original) The system according to claim 21, further comprising:

said memory controller being coupled to a service processor utilizing a JTAG bus.

23-24. (Canceled)

25. (Currently amended) A computer program product that is stored on a tangible computer readable medium in a data processing system for isolating a defect in a memory system to a particular memory system component, said product comprising:

said memory card coupled to said memory controller using a JTAG bus, said memory card including a plurality of empty slots to which additional physical DIMMs can be attached, and said memory card including a plurality of electrical buffers that are part of said memory card;

instructions for testing said plurality of physical DIMMs first using a physical DIMM test;

responsive to no error occurring during said physical DIMM test, instructions for testing said memory card using a memory card test;

responsive to no error occurring during said memory card test, instructions for testing said memory controller next using a memory controller test;

responsive to said memory controller passing said memory controller test, instructions for determining that said memory system is good;

instructions for utilizing said plurality of electrical buffers as a virtual memory controller when testing said plurality of physical DIMMs, and utilizing said plurality of electrical buffers as virtual physical DIMMs when testing said memory card;

coupling said plurality of electrical buffers to a service processor using a JTAG bus, said service processor controlling said plurality of electrical buffers using said JTAG bus;

said physical DIMM test including:

instructions for scanning DIMM test data and address information to said plurality of electrical buffers, which then scan said DIMM test data to all addresses in each one of said plurality of physical DIMMs;

instructions for reading data from said plurality of physical DIMMs;

instructions for scanning, from said plurality of electrical buffers, said data that was read from said plurality of physical DIMMs;

instructions for determining that said plurality of physical DIMMs passed said physical DIMM test if said data that was read from said plurality of physical DIMMs matches said DIMM test data;

said memory card test including:

instructions for assigning a unique identifier to each one of said plurality of electrical buffers, each one of said plurality of electrical buffers addressable by the service processor using said unique identifier;

instructions for treating each one of said plurality of electrical buffers as a virtual physical DIMM;

instructions for testing, by the service processor, data bits by writing card test data to each memory location in said virtual physical DIMM, and then reading data from each memory location in said virtual physical DIMM;

if said data that was read from said virtual physical DIMM matches said card test data, instructions for performing address bit verification on said memory card;

said address bit verification to test address bits including:

instructions for writing a known test pattern to a first memory location that falls within a range of said virtual physical DIMM, and then reading a set of addresses that fall within said range of said virtual physical DIMM;

instructions for determining whether said known test pattern was read from only said first memory location;

if said known test pattern was read from only said first memory location; said service processor determining that said memory card passed said address bit verification for said first memory location, removing said known test pattern from said first memory location, and performing said address bit verification on a next memory location; and

if all memory locations that fall within said range pass said address bit verification, instructions for determining that said memory card passed said memory card test.

~~said memory system including a plurality of components, said plurality of components including a physical memory module coupled to a memory card;~~

~~said memory card, and a memory controller for controlling said memory card; and~~

~~instruction means for testing each one of said plurality of components separately to identify a defective one of said plurality of components.~~

26-27. (Canceled)